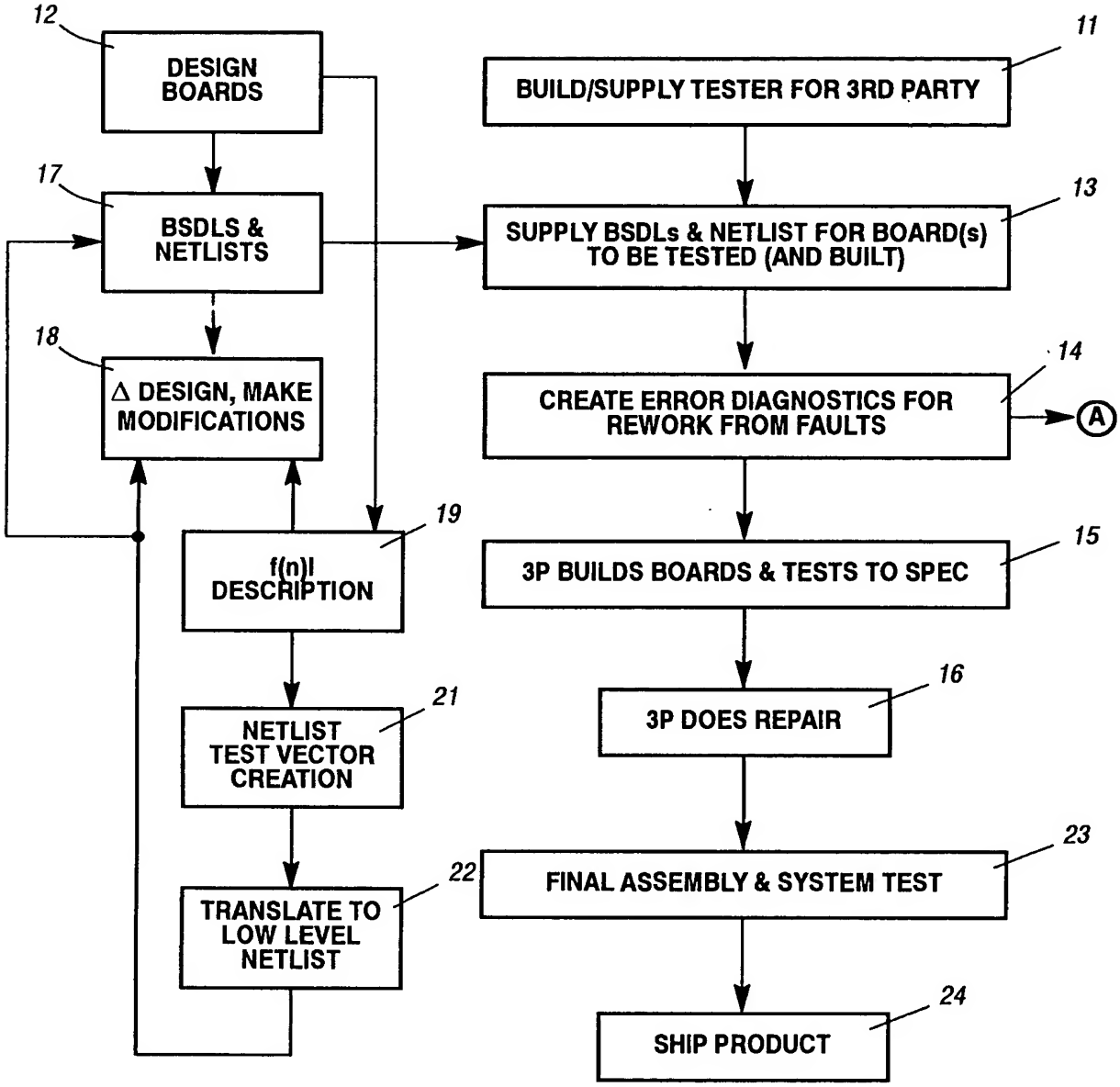

12
DESIGN BOARDS
17
BSDLS & NETLISTS
18
Δ DESIGN, MAKE MODIFICATIONS
19
f(n)l DESCRIPTION
21
NETLIST TEST VECTOR CREATION
22
TRANSLATE TO LOW LEVEL NETLIST
11
BUILD/SUPPLY TESTER FOR 3RD PARTY
13
SUPPLY BSDLs & NETLIST FOR BOARD(s) TO BE TESTED (AND BUILT)
14
CREATE ERROR DIAGNOSTICS FOR REWORK FROM FAULTS
A
15
3P BUILDS BOARDS & TESTS TO SPEC
16
3P DOES REPAIR
23
FINAL ASSEMBLY & SYSTEM TEST
24
SHIP PRODUCT
10

Figure 1

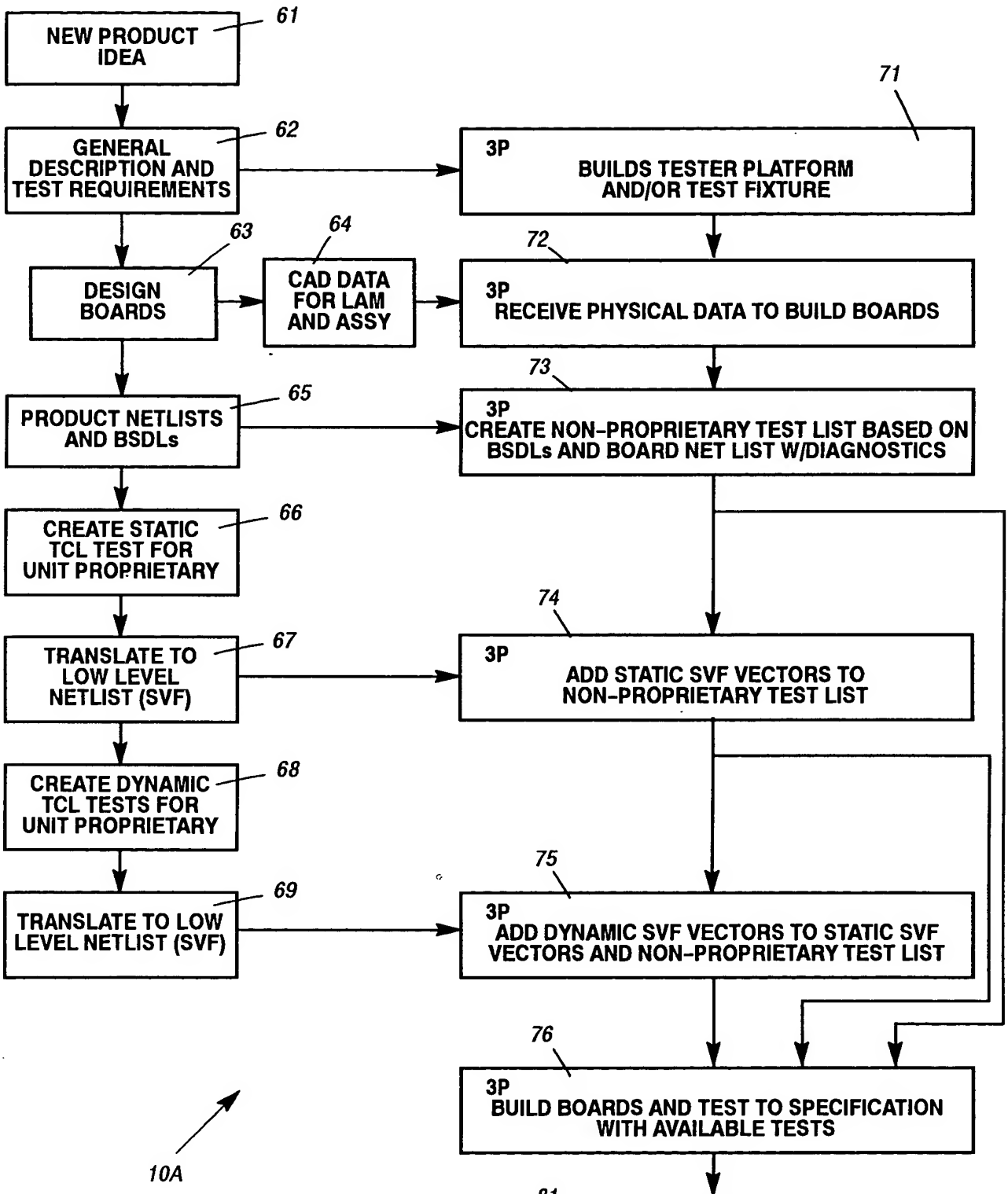

NEW PRODUCT IDEA
61
GENERAL DESCRIPTION AND TEST REQUIREMENTS
62
DESIGN BOARDS
63
CAD DATA FOR LAM AND ASSY
64
PRODUCT NETLISTS AND BSDLs
65
CREATE STATIC TCL TEST FOR UNIT PROPRIETARY
66
TRANSLATE TO LOW LEVEL NETLIST (SVF)
67
CREATE DYNAMIC TCL TESTS FOR UNIT PROPRIETARY
68
TRANSLATE TO LOW LEVEL NETLIST (SVF)
69
10A
71
3P
BUILDS TESTER PLATFORM AND/OR TEST FIXTURE
72
3P
RECEIVE PHYSICAL DATA TO BUILD BOARDS
73
3P
CREATE NON-PROPRIETARY TEST LIST BASED ON BSDLs AND BOARD NET LIST W/DIAGNOSTICS
74
3P
ADD STATIC SVF VECTORS TO NON-PROPRIETARY TEST LIST
75
3P
ADD DYNAMIC SVF VECTORS TO STATIC SVF VECTORS AND NON-PROPRIETARY TEST LIST
76
3P
BUILD BOARDS AND TEST TO SPECIFICATION WITH AVAILABLE TESTS
81
FINAL ASSEMBLY & SYSTEM TEST
82
SHIP PRODUCT

Figure 1A

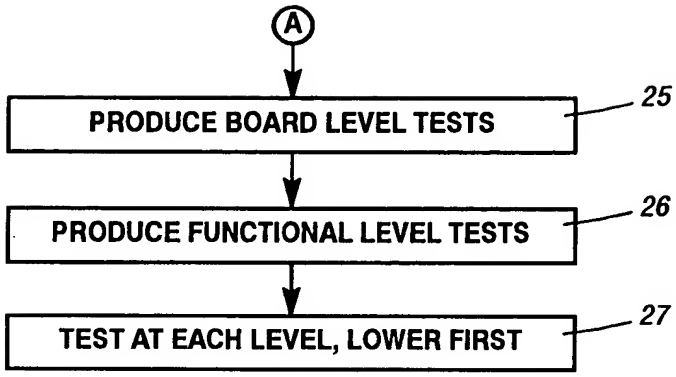

A
PRODUCE BOARD LEVEL TESTS
25
PRODUCE FUNCTIONAL LEVEL TESTS
26
TEST AT EACH LEVEL, LOWER FIRST
27

Figure 2

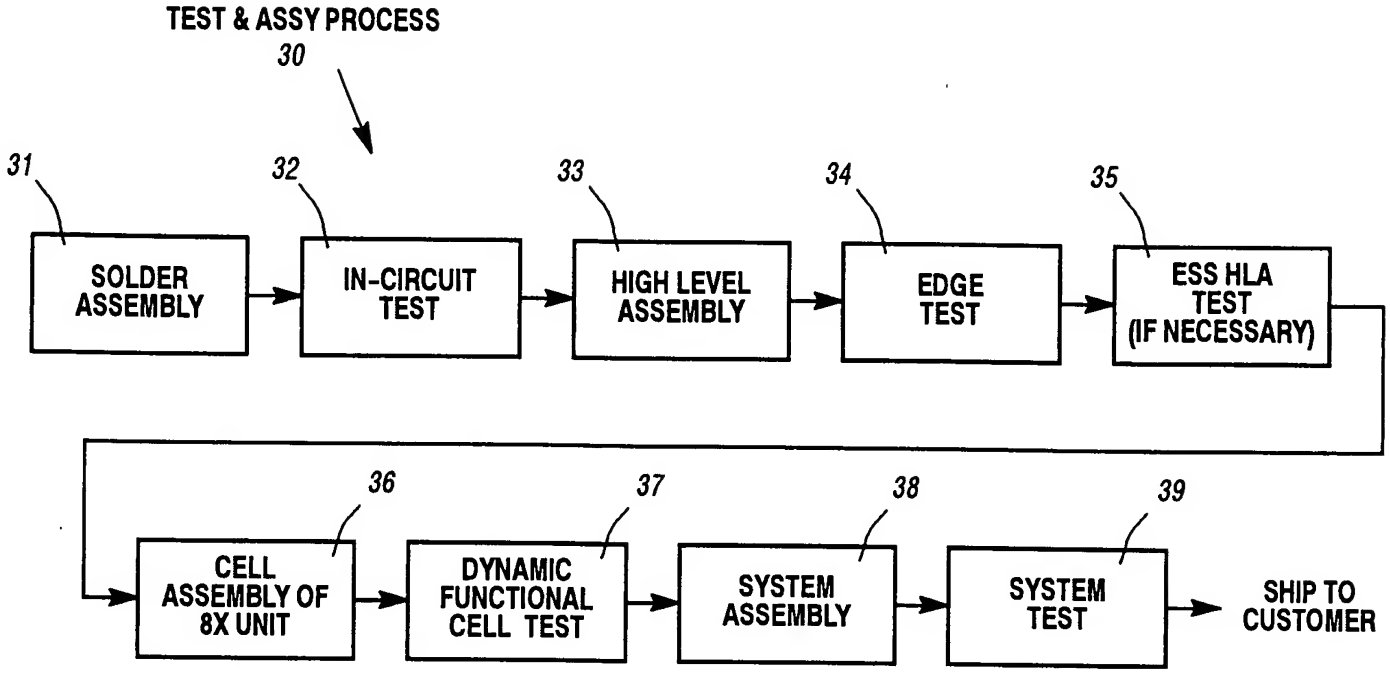

TEST & ASSY PROCESS
30
31
SOLDER ASSEMBLY
32
IN-CIRCUIT TEST
33
HIGH LEVEL ASSEMBLY
34
EDGE TEST
35
ESS HLA TEST (IF NECESSARY)
36
CELL ASSEMBLY OF 8X UNIT
37
DYNAMIC FUNCTIONAL CELL TEST
38
SYSTEM ASSEMBLY
39
SYSTEM TEST
SHIP TO CUSTOMER

Figure 3

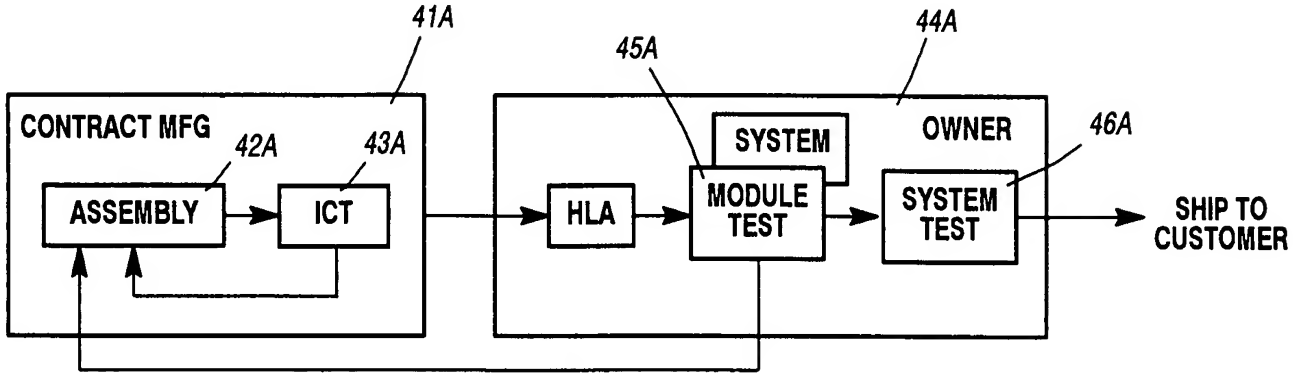
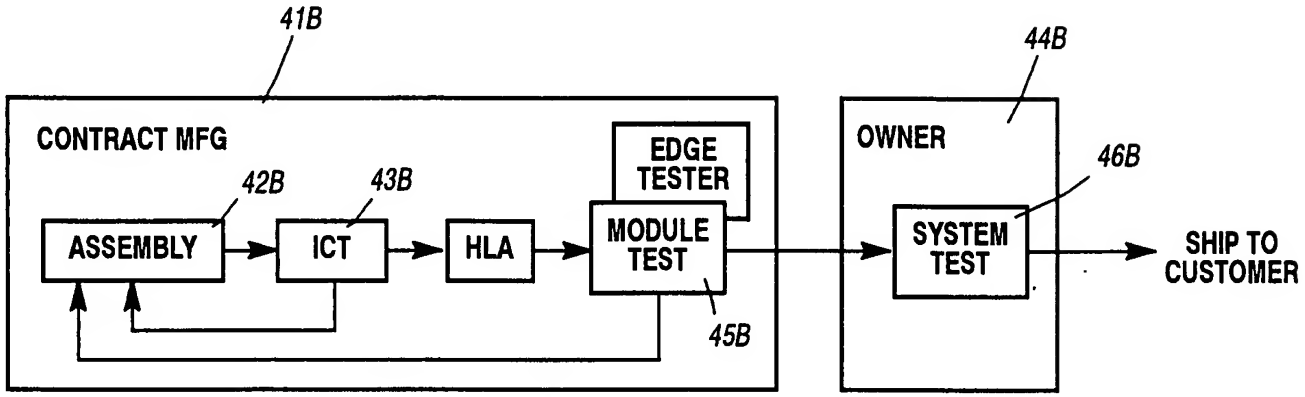


Figure 4A

Prior Art



FASTER FEEDBACK (DECREASED INVENTORY, QUICKER LEARNING, BETTER YIELD)
IMPROVED DATA COLLECTION

Figure 4B

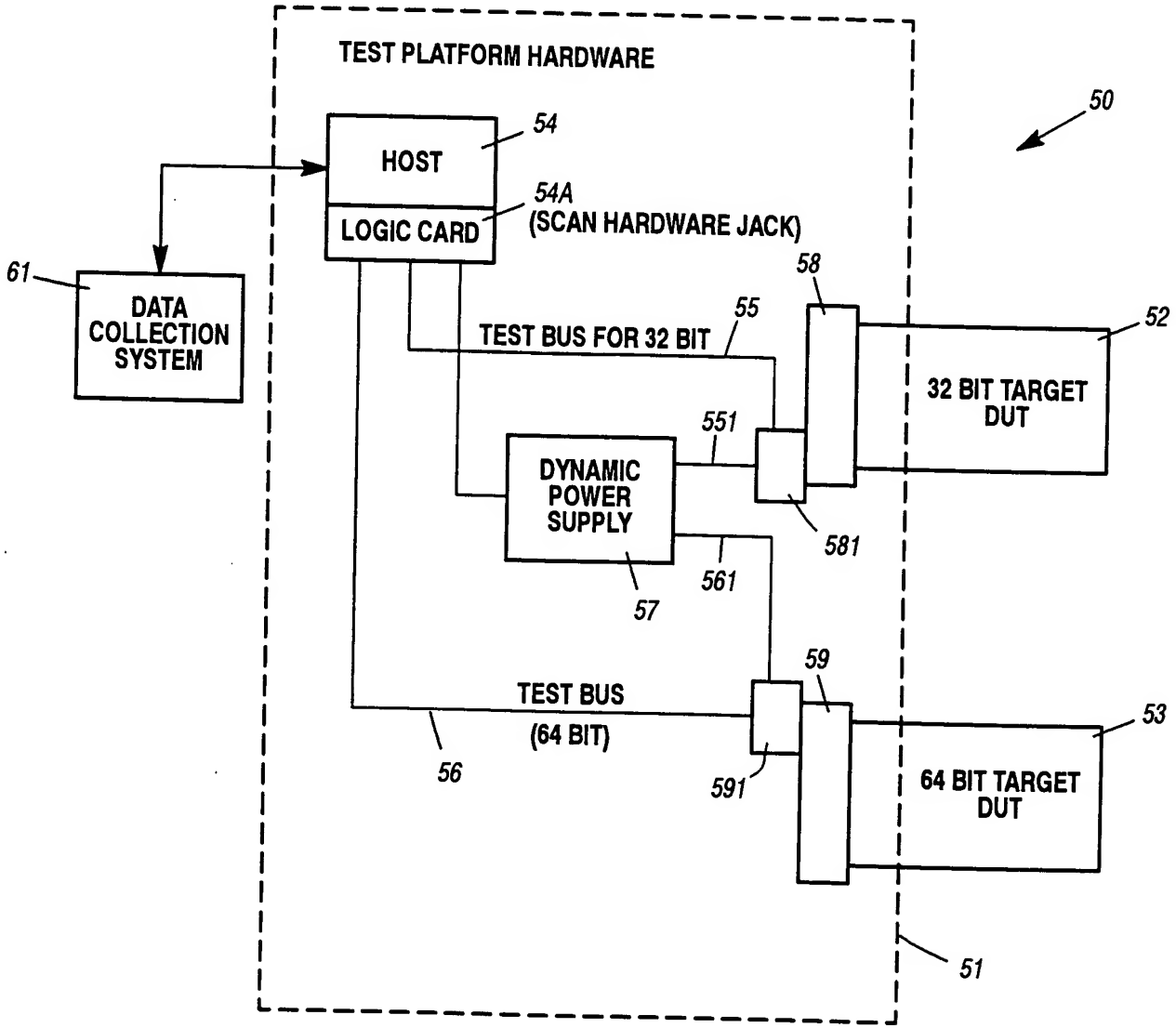

TEST PLATFORM HARDWARE
50
HOST
54
54A
LOGIC CARD
(SCAN HARDWARE JACK)
61
DATA COLLECTION SYSTEM
58
55
TEST BUS FOR 32 BIT
52
32 BIT TARGET DUT
551
DYNAMIC POWER SUPPLY
581
561
57
59
TEST BUS
(64 BIT)
53
56
591
64 BIT TARGET DUT
51

Figure 5A

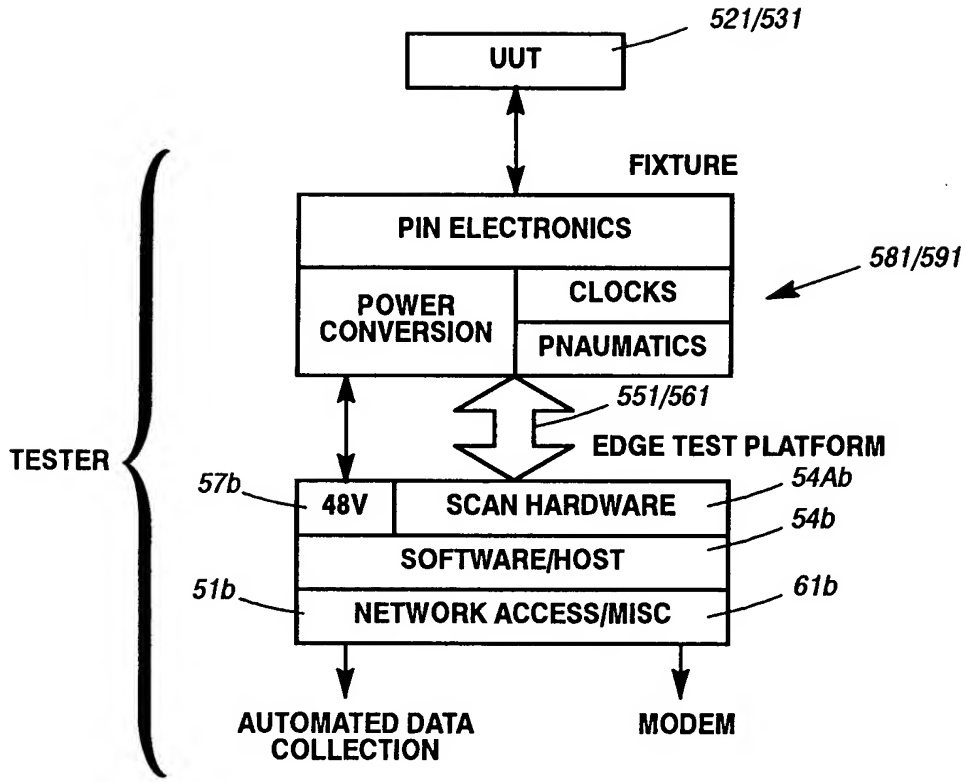

521/531
UUT
FIXTURE
PIN ELECTRONICS
581/591
POWER CONVERSION
CLOCKS
PNAUMATICS
551/561
EDGE TEST PLATFORM
TESTER
57b
48V
SCAN HARDWARE
54Ab
54b
SOFTWARE/HOST
51b
NETWORK ACCESS/MISC
61b
AUTOMATED DATA COLLECTION
MODEM

Figure 5B

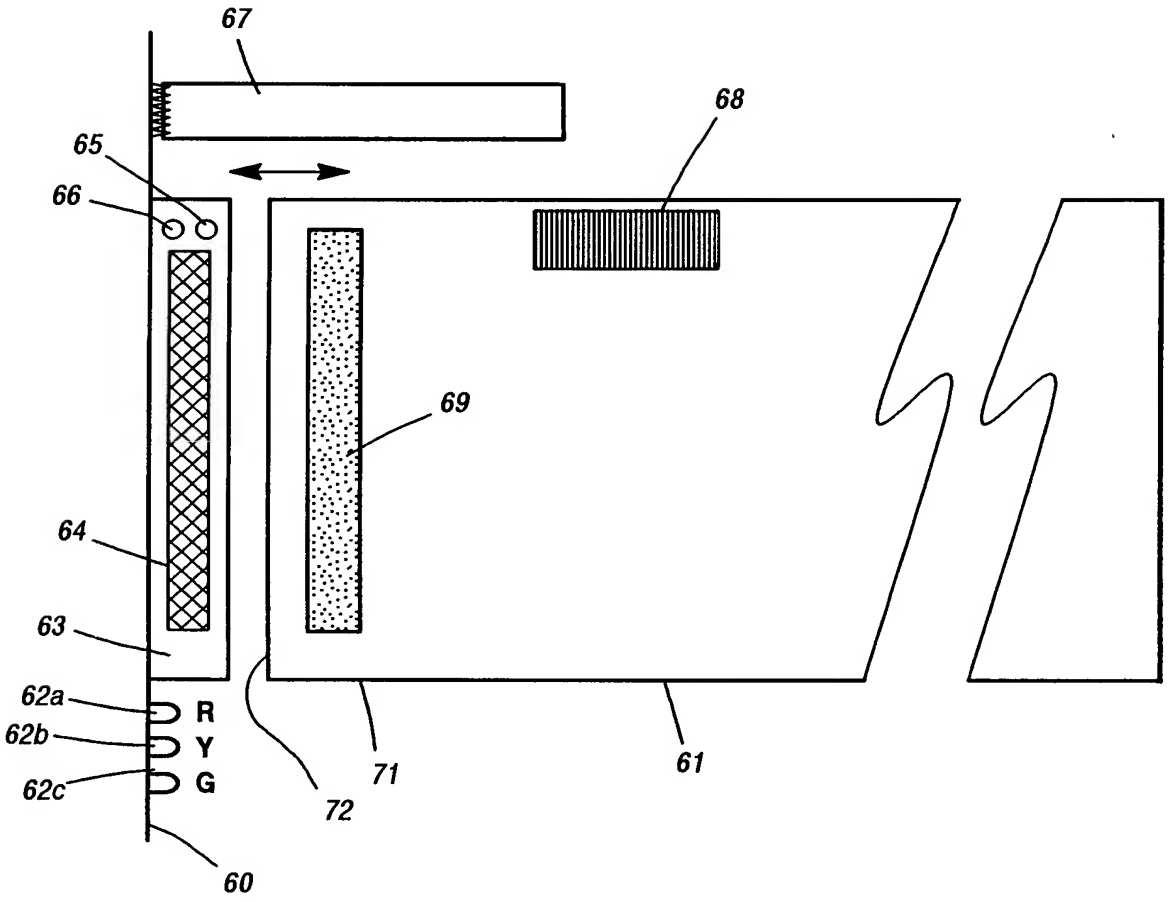


Figure 6

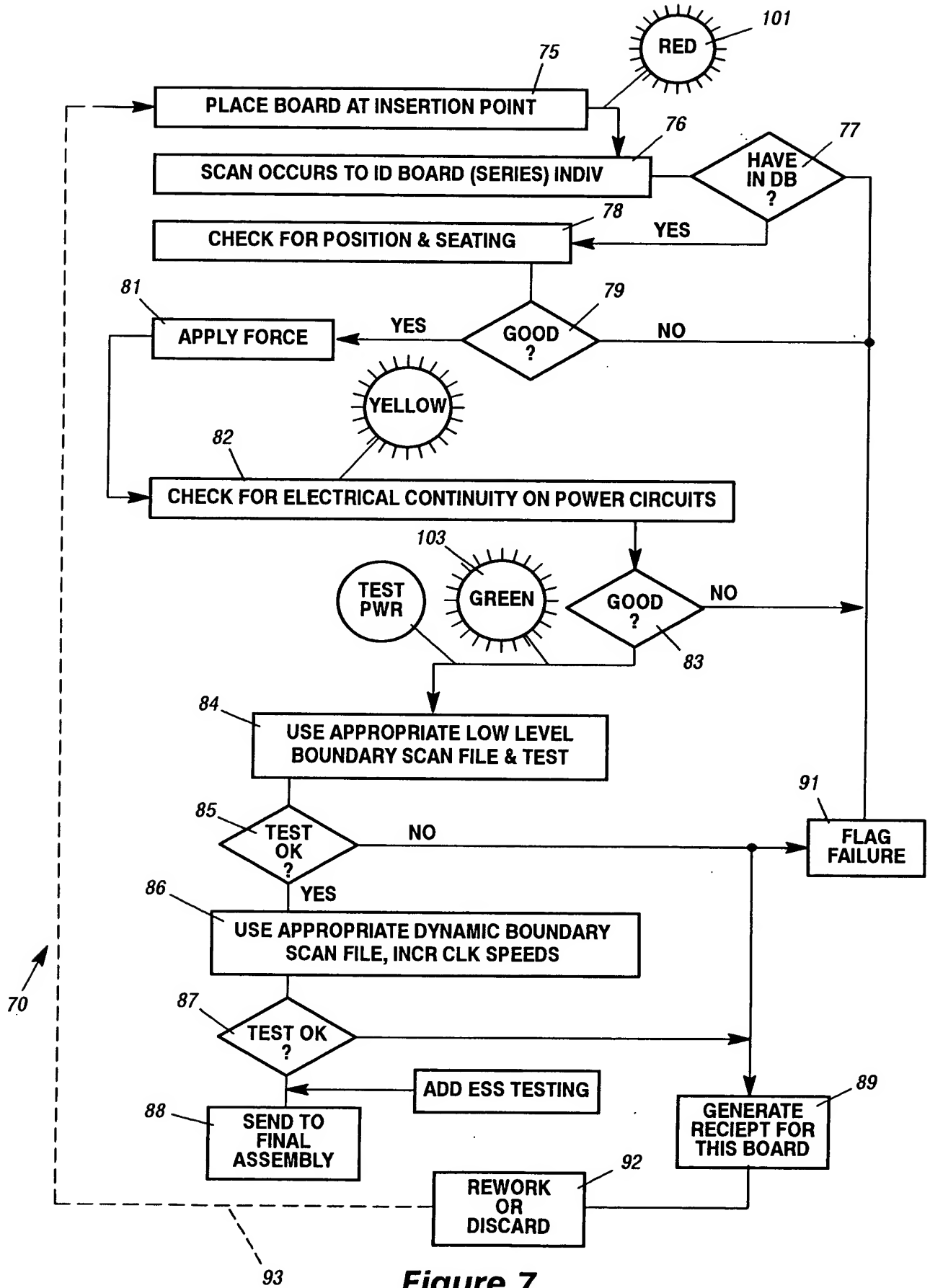
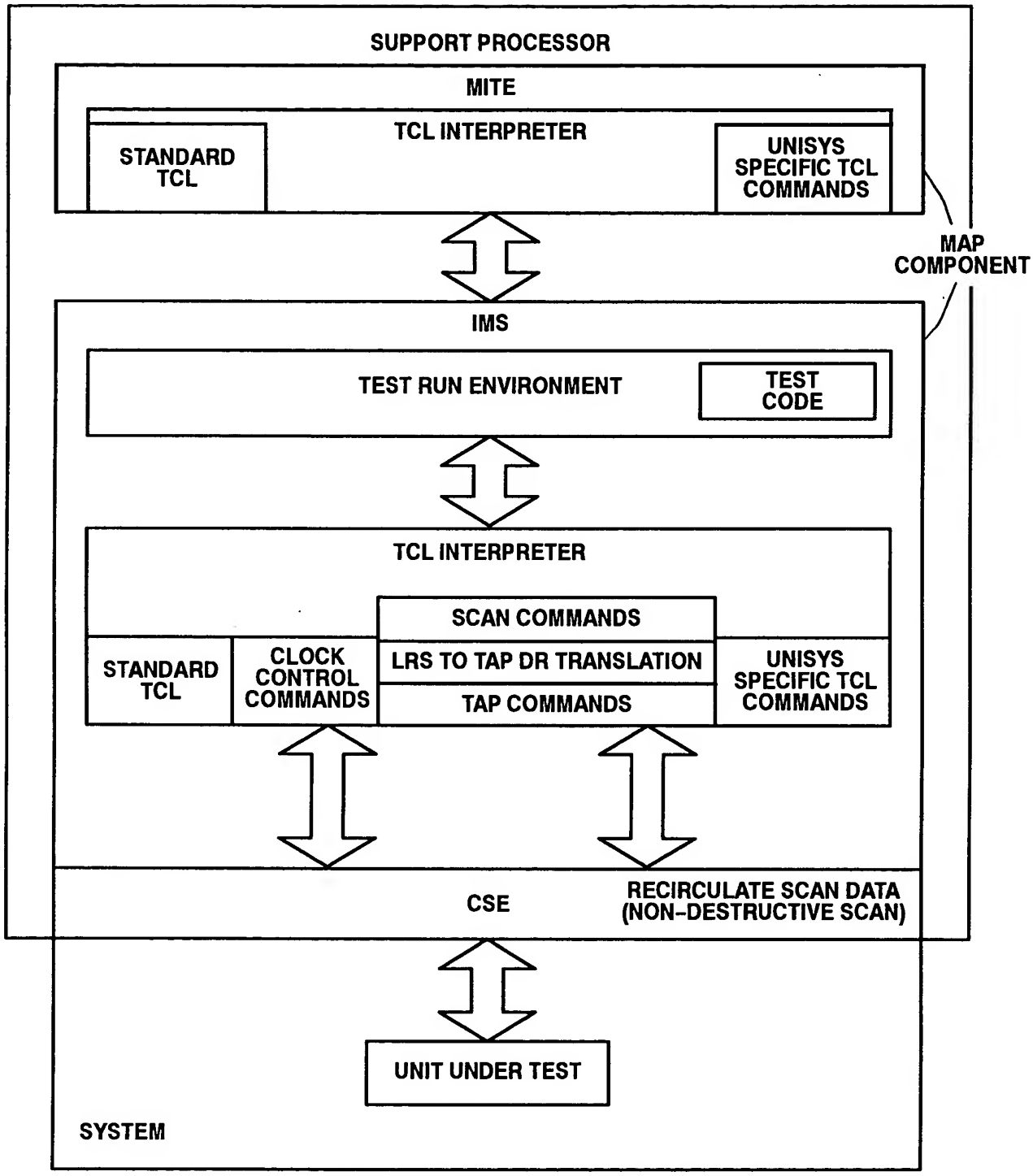
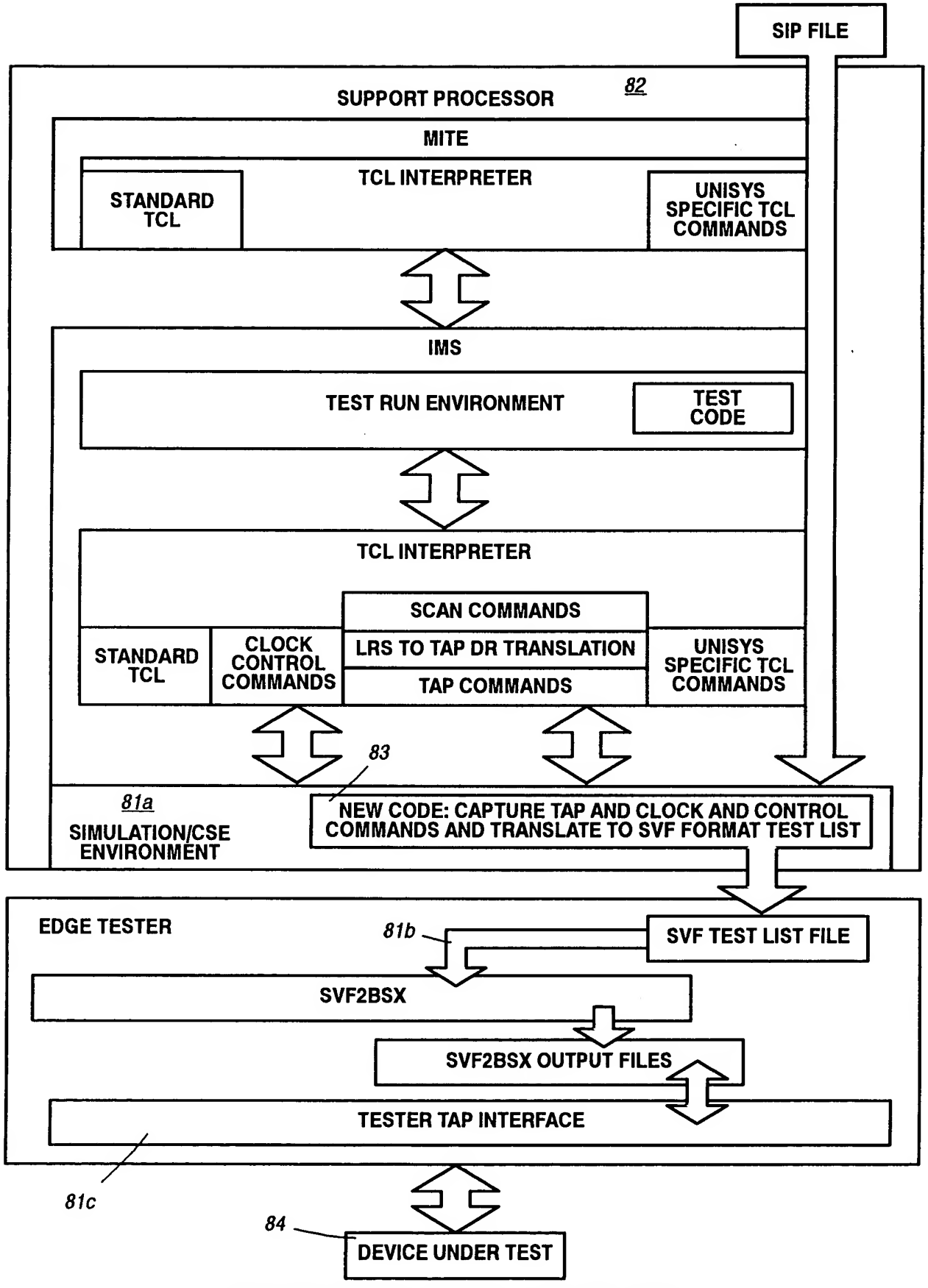

RED
101
75
PLACE BOARD AT INSERTION POINT
76
SCAN OCCURS TO ID BOARD (SERIES) INDIV
77
HAVE IN DB ?
YES
78
CHECK FOR POSITION & SEATING
81
APPLY FORCE
YES
79
GOOD ?
NO
YELLOW
82
CHECK FOR ELECTRICAL CONTINUITY ON POWER CIRCUITS
103
TEST PWR
GREEN
GOOD ?
NO
83
84
USE APPROPRIATE LOW LEVEL BOUNDARY SCAN FILE & TEST
91
85
TEST OK ?
NO
FLAG FAILURE
YES
86
USE APPROPRIATE DYNAMIC BOUNDARY SCAN FILE, INCR CLK SPEEDS
87
TEST OK ?
ADD ESS TESTING
89
GENERATE RECIEPT FOR THIS BOARD
88
SEND TO FINAL ASSEMBLY
92
REWORK OR DISCARD
70
93

Figure 7



(IN-HOUSE TESTING)

Figure 8A



(THIRD PARTY-ENABLED TESTING)

Figure 8B

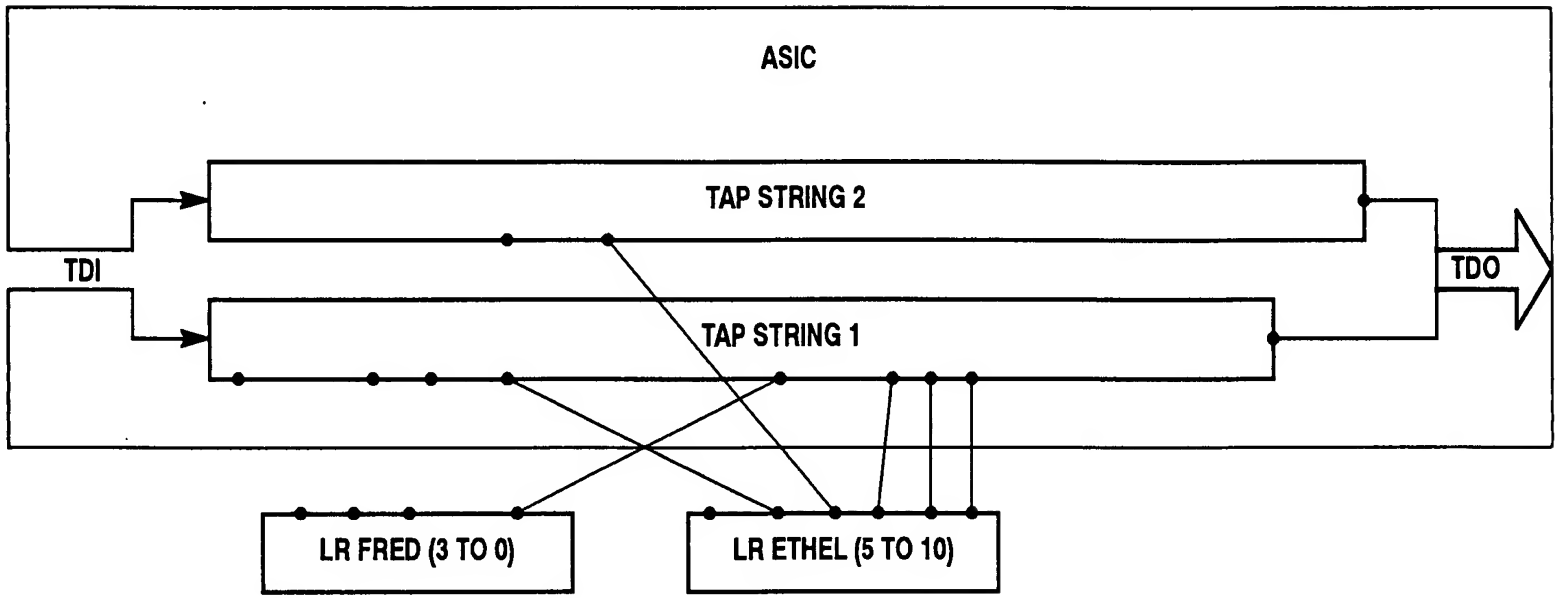
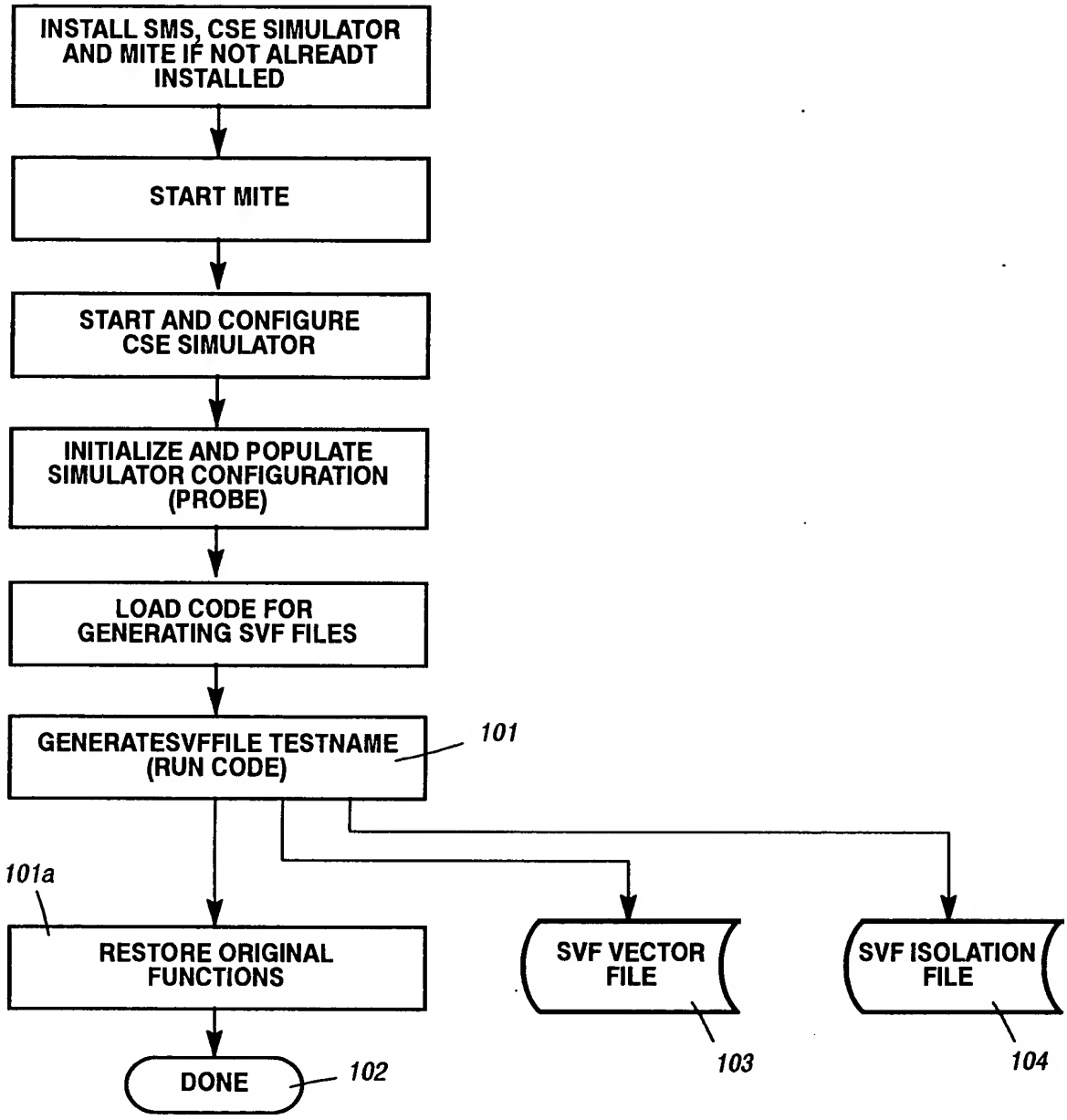
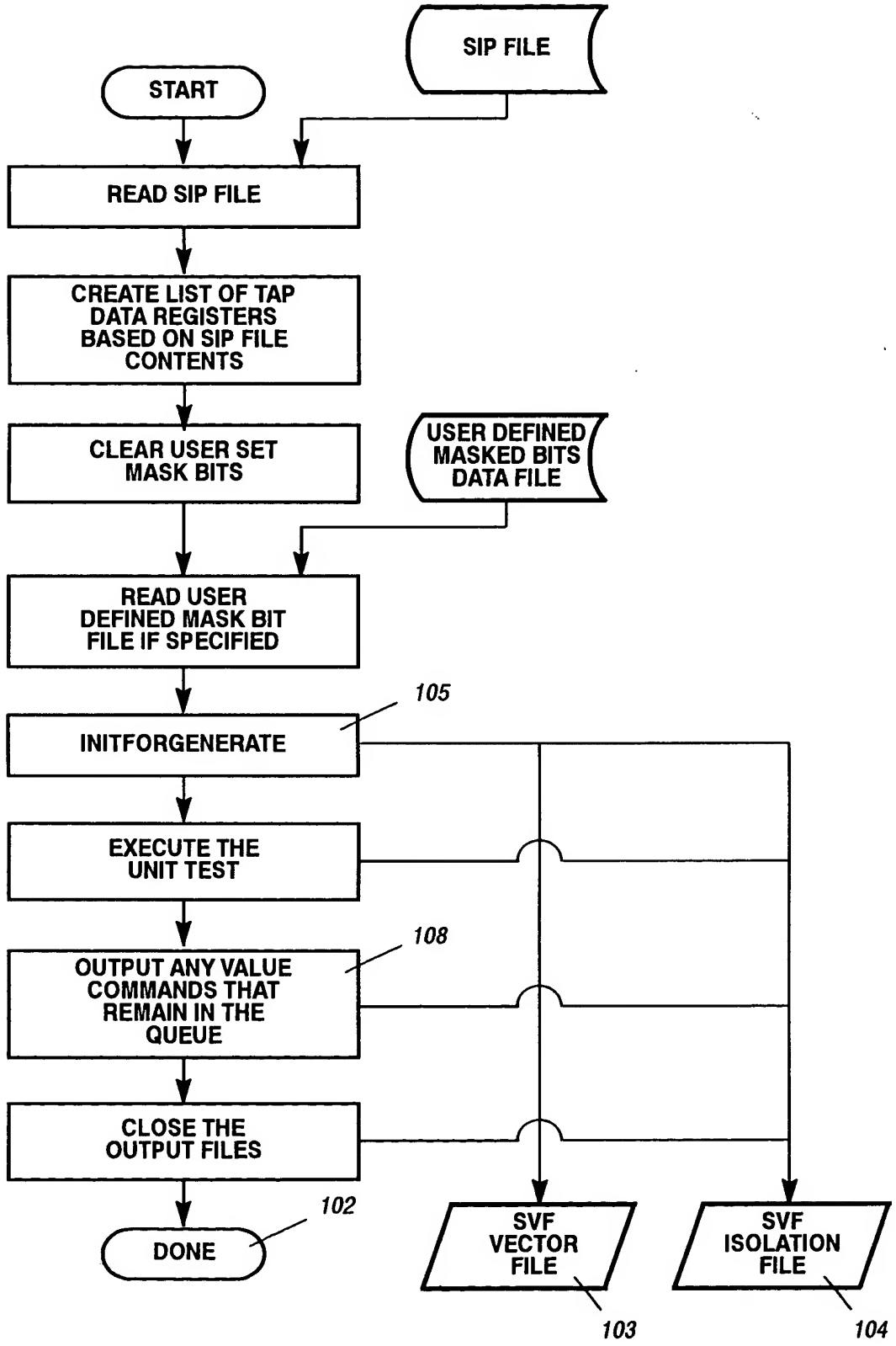

ASIC
TAP STRING 2
TDI
TDO
TAP STRING 1
LR FRED (3 TO 0)
LR ETHEL (5 TO 10)

Figure 9



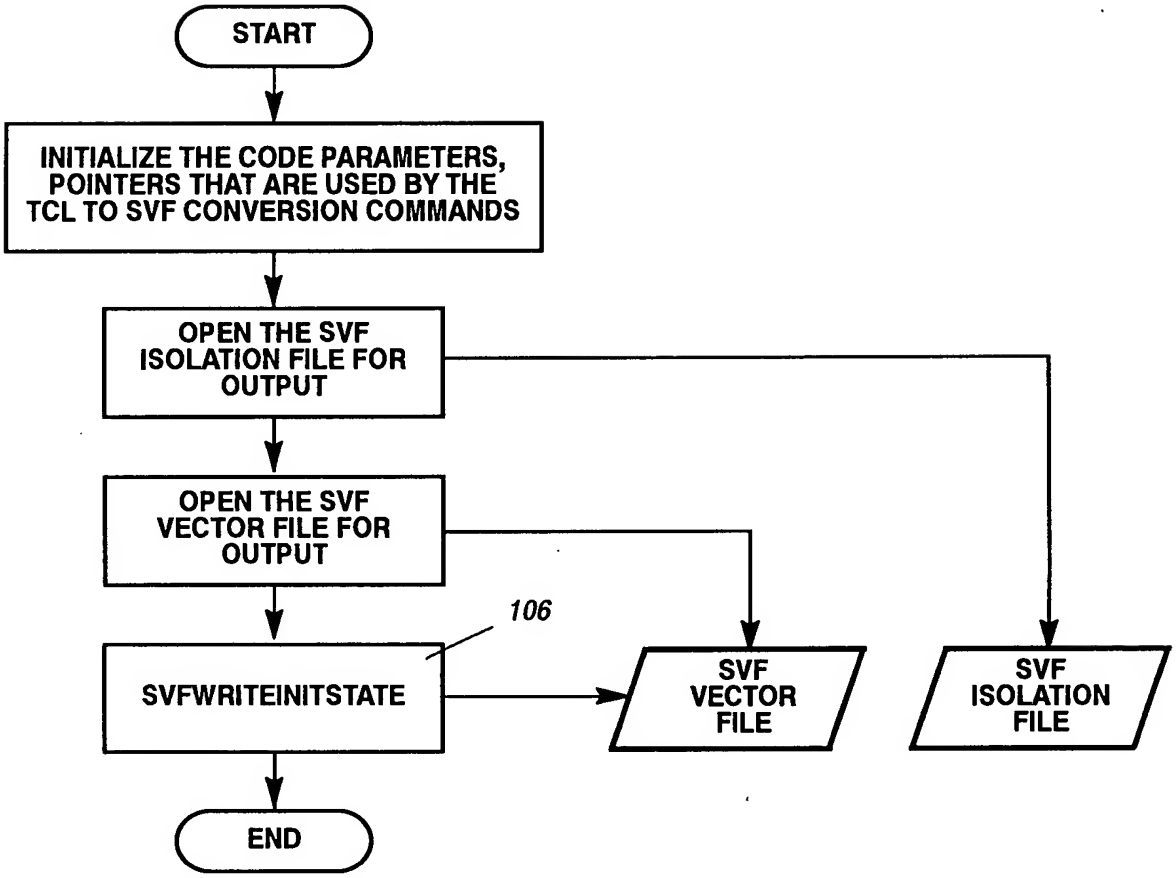
UNIT TEST TO SVF FORMAT CONVERSION PROCESS

Figure 10A



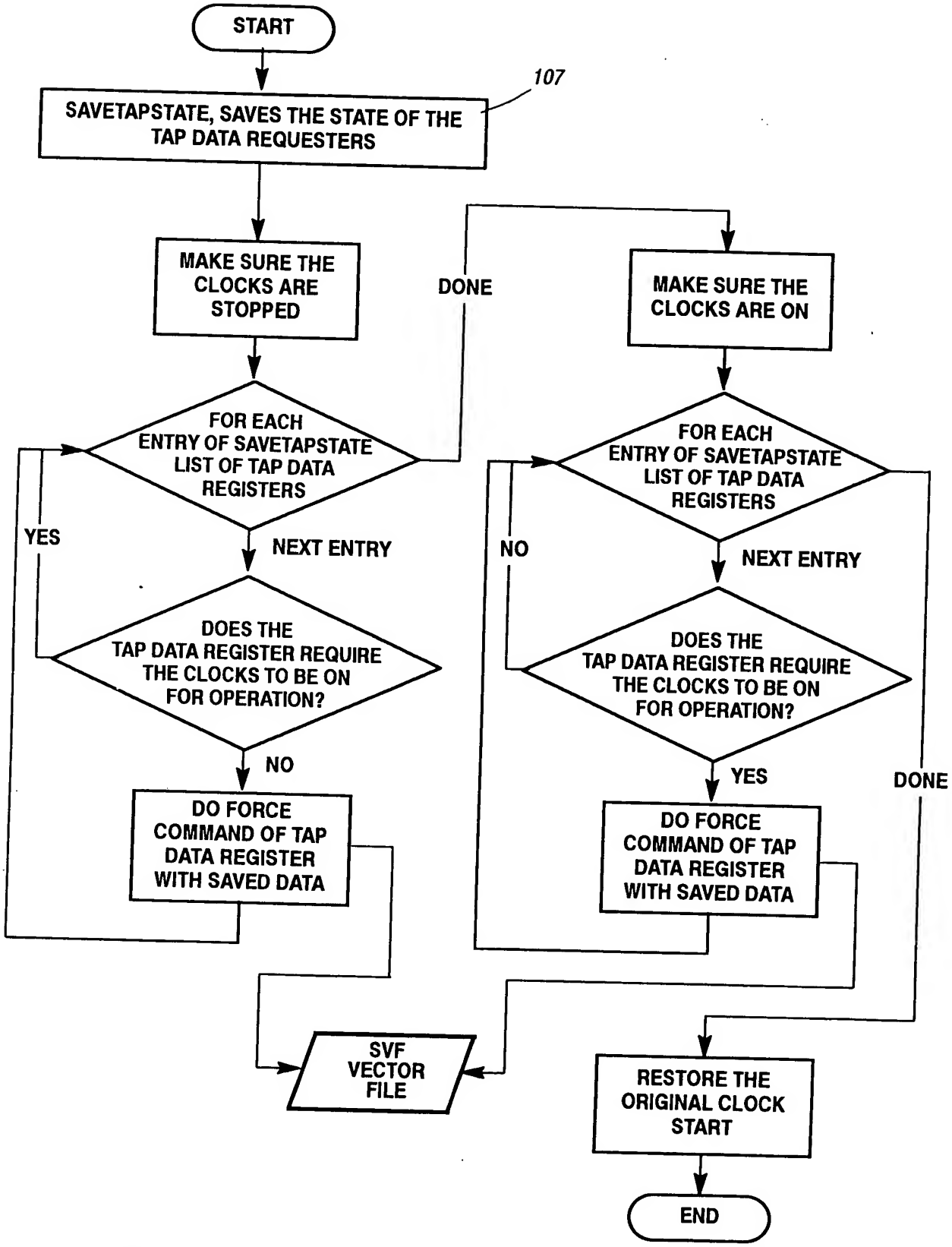
GENERATESVFFILE FLOWCHART

Figure 10B



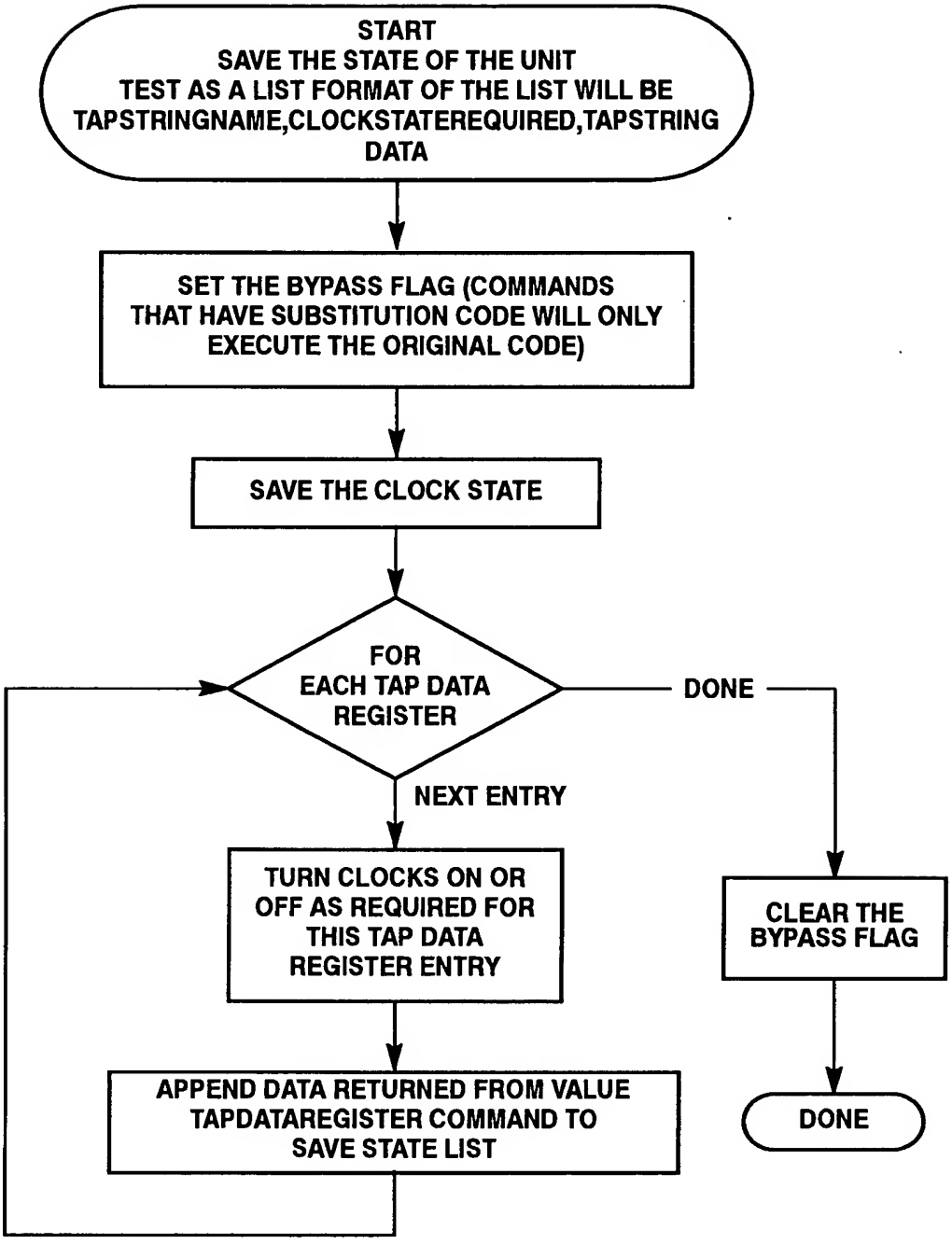
TCL CODE FOR INITFORGENERATE COMMAND FOR TCL TO SVF FORMAT CONVERSION

Figure 10C



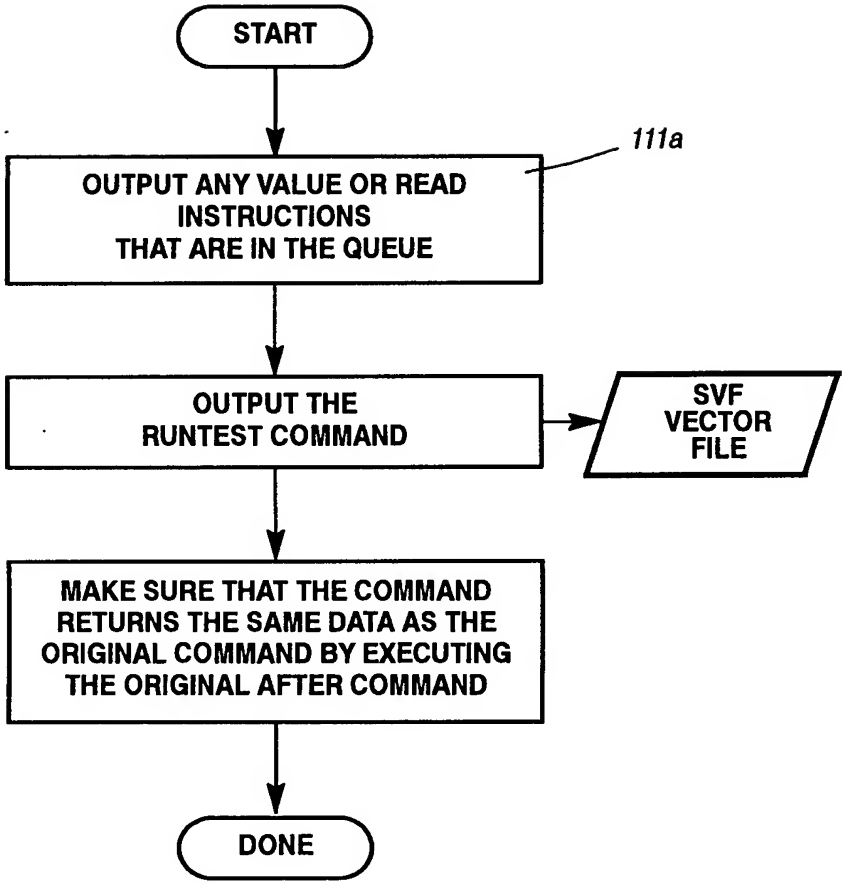
TCL WRITEINITSTATE COMMAND FOR SVF TO TCL CONVERSION

Figure 10D



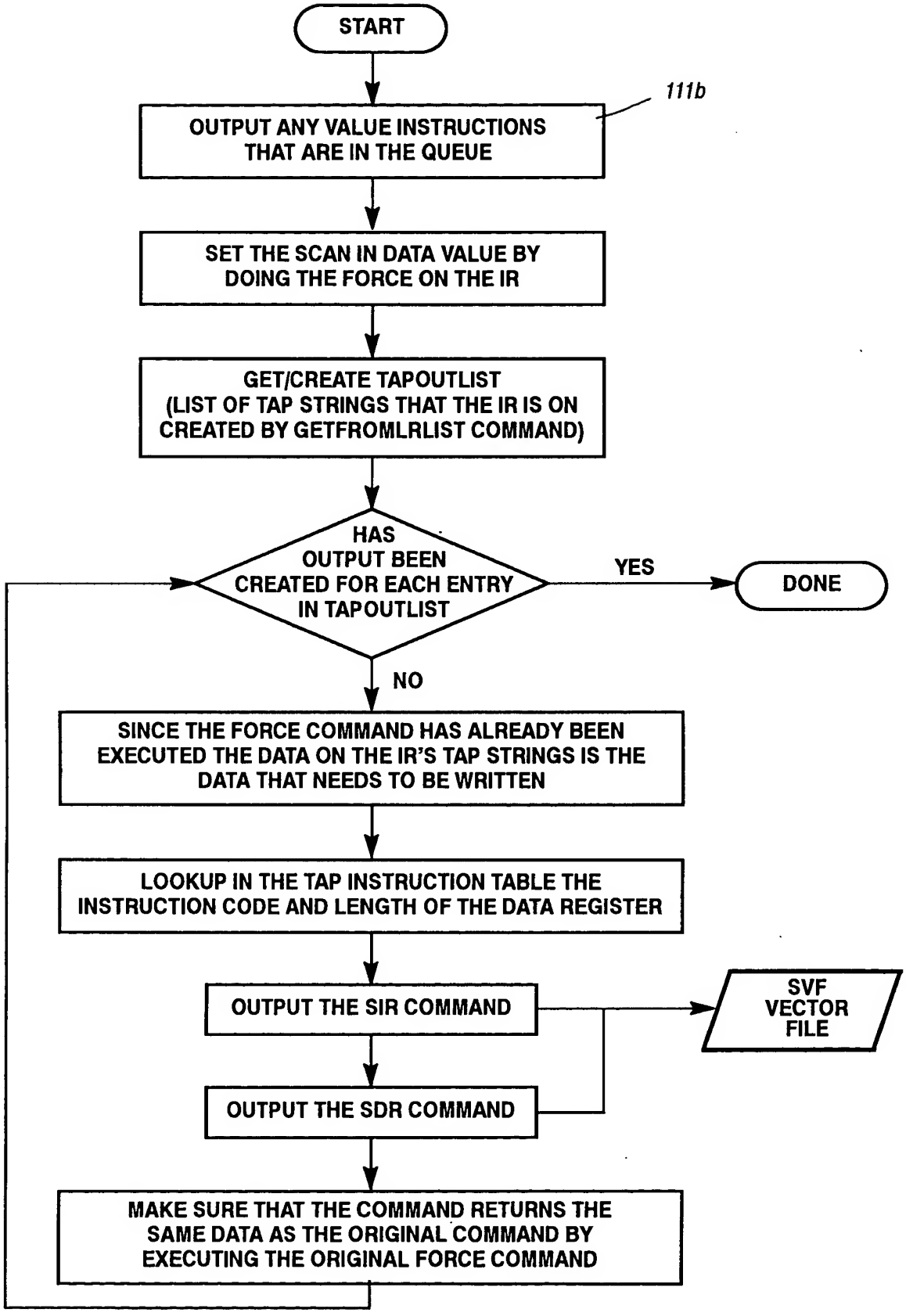
SAVE STATE TEL COMMAND FOR TEL TO SVF CONVERSION

Figure 10E



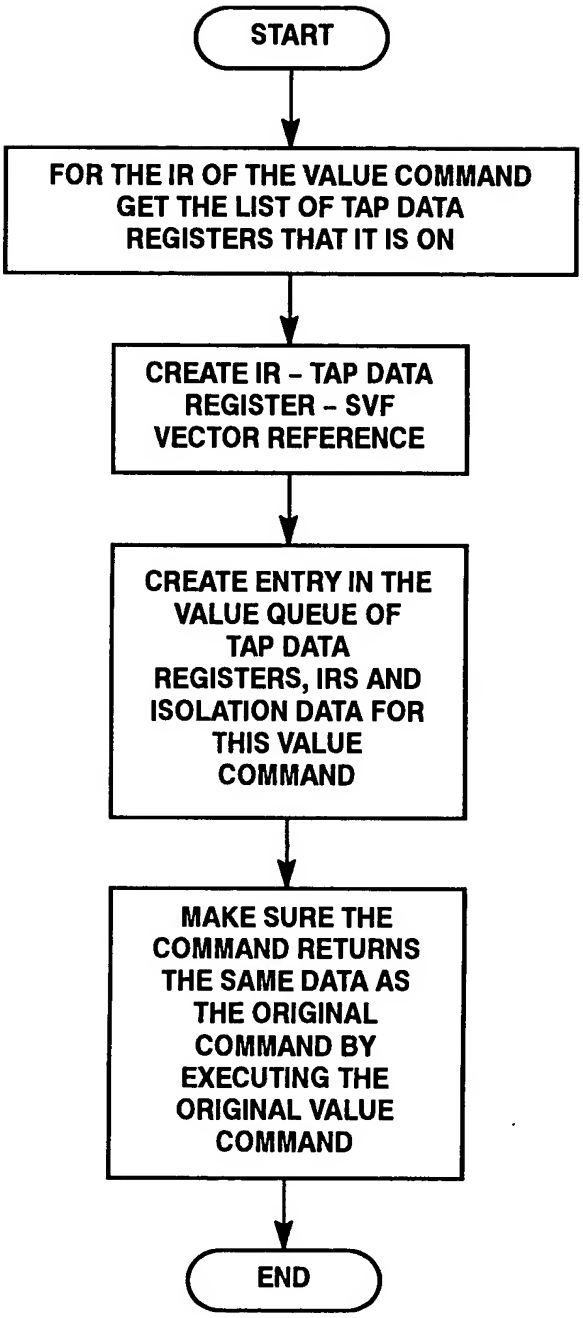
TCL CODE TO CONVERT AFTER COMMAND TO SVF FORMAT

Figure 10F



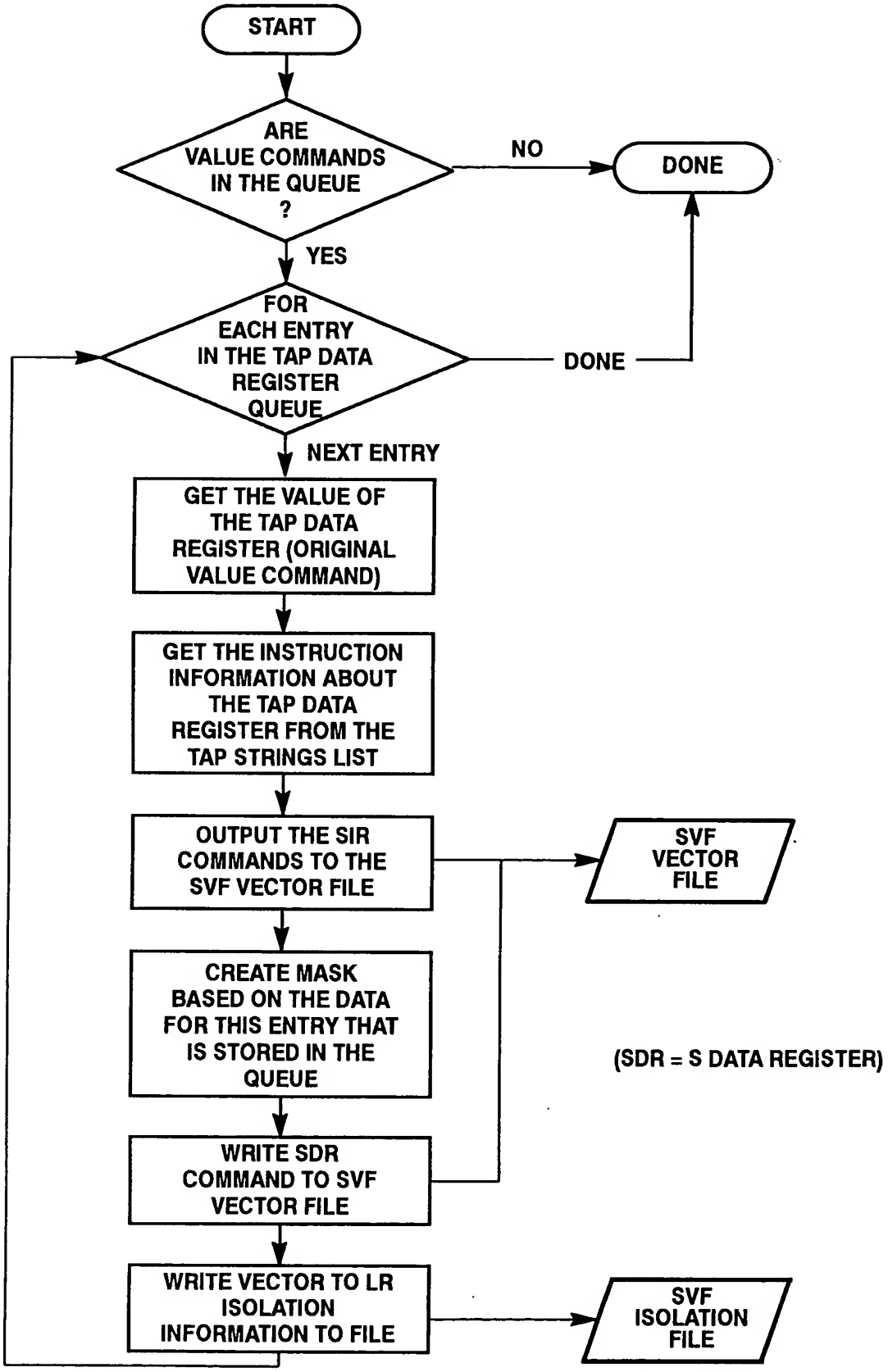
TCL CODE TO CONVERT FORCE COMMAND TO SVF FORMAT

Figure 10G



TCL CODE TO CONVERT VALUE COMMAND TO SVF FORMAT

Figure 10H



EXPANSION OF OUTPUT VALUE INSTRUCTIONS IN QUEUE (IIIa AND IIIb) FROM FIG. 10F AND 10G

Figure 10I

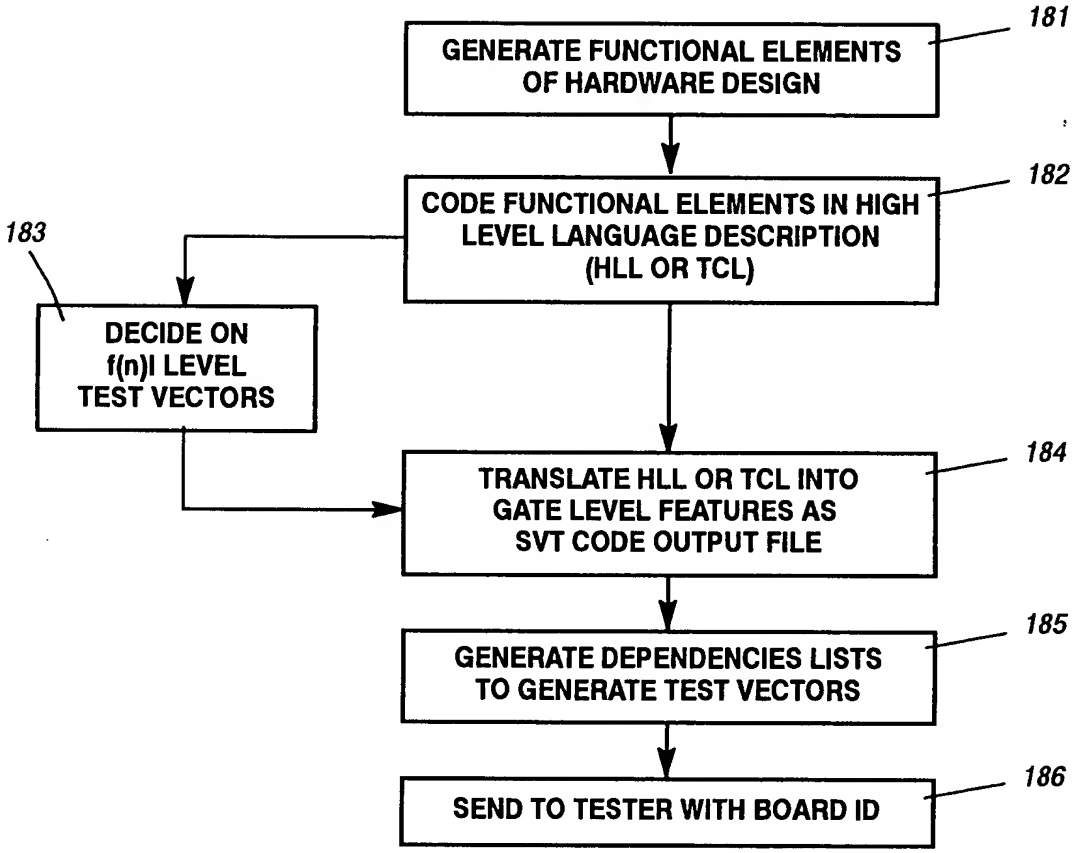

GENERATE FUNCTIONAL ELEMENTS OF HARDWARE DESIGN
181
CODE FUNCTIONAL ELEMENTS IN HIGH LEVEL LANGUAGE DESCRIPTION (HLL OR TCL)
182
183
DECIDE ON f(n)I LEVEL TEST VECTORS
TRANSLATE HLL OR TCL INTO GATE LEVEL FEATURES AS SVT CODE OUTPUT FILE
184
GENERATE DEPENDENCIES LISTS TO GENERATE TEST VECTORS
185
SEND TO TESTER WITH BOARD ID
186

Figure 11